REMARKS

This amendment is in response to the Office action mailed on 12 December 2003.

Claims 1-16 were presented for examination. Claims 1-3 and 11-16 were rejected. Claims 5-10 were objected to as being dependent on a rejected base claim. Claims 1-16 have been canceled, and new claims 17-27 are presented in this amendment. The applicant respectfully requests reconsideration in light of the following comments.

35 U.S.C. 112 Rejection of Claim 1

Claim 1 was rejected under 35 U.S.C. 112, second paragraph, as containing an internal conflict. Claim 1 has been canceled. The applicant respectfully submits that the new claims are allowable.

35 U.S.C. 103 Rejection of Claims 1, 2, 3, 11-14, and 16

Claims 1, 2, 3, 11-14, and 16 were rejected under 35 U.S.C. 103(a) as unpatentable over Lowell et al., U.S. Patent No. 3,623,017 (hereinafter "Lowell") in view of Hofmann et al., U.S. Patent No. 6,504,854 (hereinafter "Hofmann"). The applicant respectfully submits that the claims, as amended, overcome the rejection and are allowable.

New claim 17 recites:

> 17. (new) An apparatus comprising:
>
> circuitry for sending and receiving serial input/output data at a rate equal to that of a source clock signal;
>
> an instruction decoder connected to said circuitry for controlling the operation of said apparatus based on the decoding of a specific instruction;
>
> a memory for storing instructions connected to said instruction decoder;
>
> a program counter connected to said memory and to said instruction decoder; and
>
> a function clock generator for generating a function clock signal that governs the rate of instruction execution within said apparatus, wherein said function clock generator is connected to said program counter, said instruction decoder, and said circuitry, and wherein the frequency of said function clock signal is decreased to equal the frequency of said source clock signal upon the decoding of said specific instruction.
>
> [Emphasis Added]

Nowhere does Lowell teach or suggest, alone or in combination with Hofmann, what new claim 17 recites – namely *circuitry for sending and receiving serial input/output data at a rate equal to that of a source clock signal . . . wherein the frequency of the function clock signal is decreased to equal the frequency of said source clock signal upon the decoding of a specific instruction*.

This is significant because the present invention achieves the advantages of programmability and reduced power consumption for a serial input/output interface by temporarily reducing the rate of instruction execution to be equal to the rate at which serial input/output bits are sent or received. Nowhere do the references teach or suggest that the processor speed should be decreased when input/output is being performed and raised when the input/output is over.

Because claims 18-23 depend on claim 17, the applicant respectfully submits that they are also allowable.

New claim 24 recites:

> 24. (new) A method comprising:
>
> sending and receiving serial input/output data under the control of decoded instructions, and at a rate equal to the frequency of a source clock signal;
>
> executing said instructions at a rate equal to that of the frequency of a function clock signal; and
>
> decreasing the frequency of said function clock signal to be equal to the source clock signal, based on said decoded instructions.
>
> [Emphasis Added]

Nowhere does Lowell teach or suggest, alone or in combination with Hofmann, what new claim 24 recites – namely a method comprising *sending and receiving serial input/output data under the control of decoded instructions, and at a rate equal to the frequency of a source clock signal; ... and decreasing the frequency of the function clock signal to be equal to the source clock signal, based on said decoded instructions*.

This is significant because the present invention achieves the advantages of programmability and reduced power consumption for a serial input/output interface by temporarily reducing the rate of instruction execution to be equal to the rate at which serial input/output bits are sent or received. Nowhere do the references teach or suggest that the processor speed should be decreased when input/output is being performed and raised when the input/output is over.

Because claims 25-27 depend on claim 24, the applicant respectfully submits that they are also allowable.

Request for Reconsideration Pursuant to 37 C.F.R. 1.111

Having responded to each and every ground for rejection in the Office action mailed 12 December 2003, the applicants request reconsideration of the instant application pursuant to 37 CFR 1.111 and request that the Examiner allow all of the pending claims and pass the application to issue.

Should there remain unresolved issues the applicants respectfully request that Examiner telephone the applicants' attorney at 732-578-0103 x11 so that those issues can be resolved as quickly as possible.

Respectfully,
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Date 1/5/04

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